UNIVERSITY COLLEGE OF ENGINEERING
OSMANIA UNIVERSITY, HYDERABAD
M.E. (ECE, Mech. & CSE) I - Semesters (Make-up) Examination
April 2018

Examination Centre:
Main Building
UCE (A), O.U.

MVSR ENGINEERING COLLEGE
EXAMINATION TIME TABLE
TIME : 2.00 PM TO 5.00 PM

DATE & DAY	E. C. E. (EMBEDDED SYSTEMS & VLSI DESIGN)	MECHANICAL (CAD / CAM)	C. S. E.
	I-Semester	I-Semester	I-Semester
02-04-2018 MONDAY	Analog IC Design	Product Design and Process Planning	Advanced Algorithms
04-04-2018 WEDNESDAY	Digital Signal Processors	Failure Analysis and Design	Artificial Intelligence
06-04-2018 FRIDAY	Global & Regional Navigational Satellite Systems	=====	=====
09-04-2018 MONDAY	Micro Controllers for Embedded System Design	Computer Integrated Manufacturing	Advanced Operating Systems
11-04-2018 WEDNESDAY	VLSI Design & Technology	Finite Element Techniques	Object Oriented Software Engineering
13-04-2018 FRIDAY	Advanced Digital Design with Verilog HDL	Optimization Techniques	Software Quality Testing
16-04-2018 MONDAY	======	Experimental Techniques and Data Analysis	Mobile Computing

DIRECTOR OF EVALUATION
EXAMINATION CELL